Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**GATE**

**.020” X .022**

**SOURCE**

**.020” X .023**

**.076”**

**.086”**

**BACKSIDE IS DRAIN**

**Top Material: Al**

**Backside Material: CrNiAg**

**Backside Potential: Drain**

**Mask: HEX1 60V P-Channel Gen 3**

**APPROVED BY: DK DIE SIZE .076” X .086” DATE: 5/15/23**

**MFG: INT’L RECTIFIER THICKNESS .011” P/N: IRFC9014**

**DG 10.1.2**

#### Rev B, 7/19/02